Predictable Out-of-order Execution Using Virtual Traces

Jack Whitham and Neil Audsley

December 3rd 2008

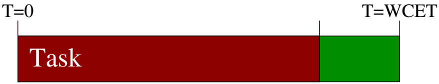
http://www.jwhitham.org.uk/c/vt.html

Topics in this talk

1. General issues with state-of-the-art worst case execution time (WCET) analysis.
2. Problem: design a CPU to reduce the WCET of a task.
3. Traces; a solution.
4. Virtual traces; a further improvement.
5. Experiments, results, observations.
6. Data scratchpads; a problem.
7. Conclusion.

State-of-the-art WCET analysis

Requirement: find an upper bound on the execution time of a task: C, the WCET.



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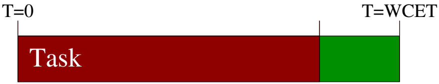

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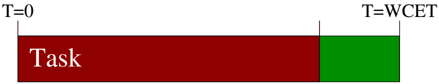

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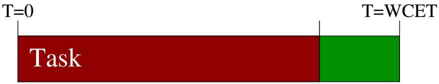

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  - pipeline modeling
    e.g. determine the worst-case state of the pipeline at point Y

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Solutions do exist for all of these problems, but they (1) raise the engineering cost and/or (2) increase the WCET.

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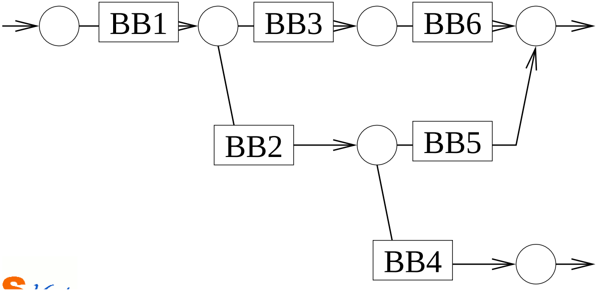
- Accommodate speculative and superscalar out-of-order operation so that throughput can be increased versus a simple CPU.
- Reduce pessimism in the WCET model.

One possibility: a trace

A trace is a path through a program, chosen to reduce C, the worst-case execution time.



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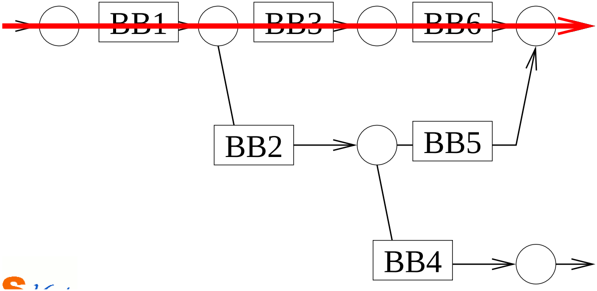

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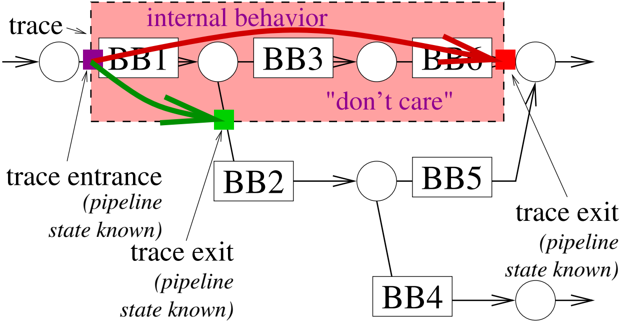

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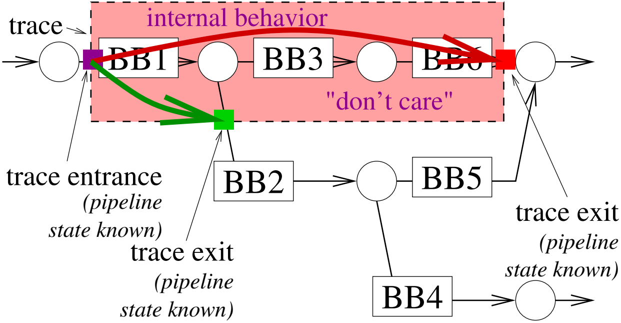

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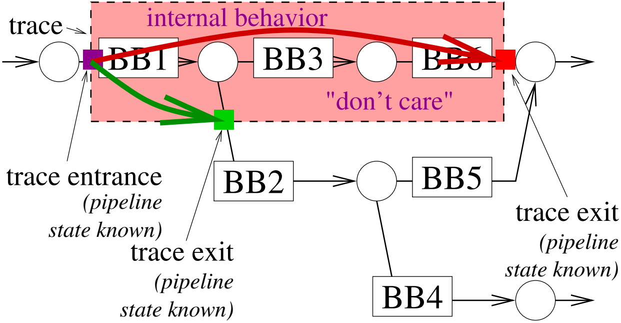

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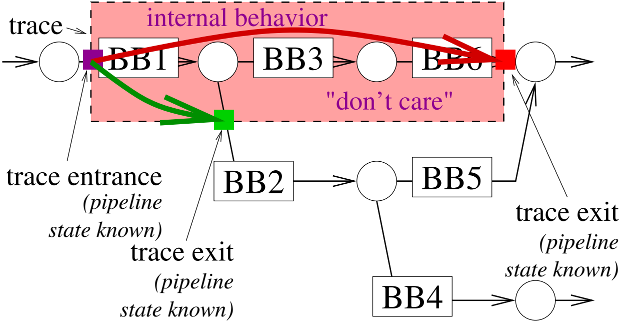
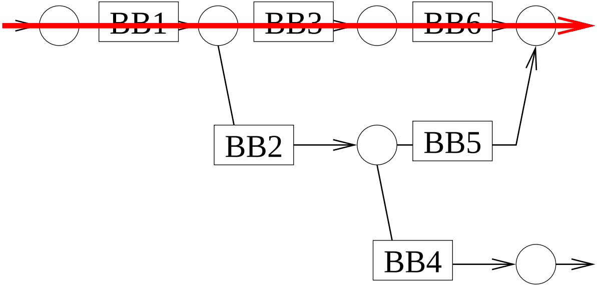


- The trace begins and ends in a known pipeline state.
- The total time for each path is exactly known (it can be measured).
- **The result:** speculation and superscalar out-of-order execution don't have to be modeled!

Static branch prediction



Contrast with *static branch prediction*. With a virtual trace, the main path has a well-defined end point, so the number of possible pipeline states is *bounded*. Static branch prediction omits this important restriction.

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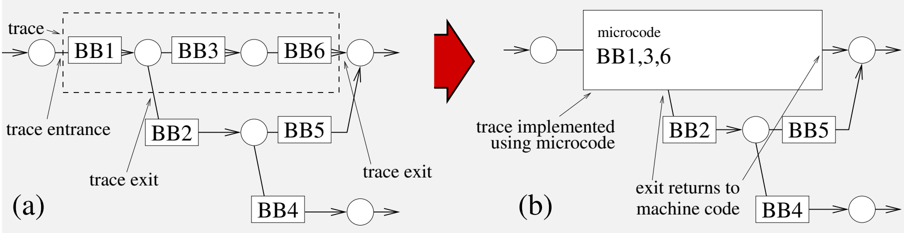
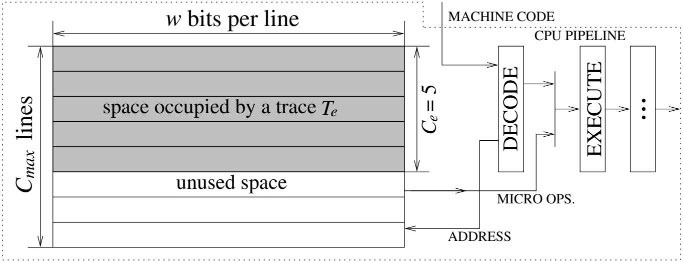


Previous work

4. Allocate space in a *trace scratchpad* for microcode.
   The microcode is used in place of the original machine code.



J. Whitham and N. Audsley, Using trace scratchpads to reduce execution times in predictable real-time architectures, Proc. RTAS, 305–316, 2008.

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- the memory space requirements of microcode.

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Virtual in the sense that the microcode is generated dynamically - we know what the scheduler will do, but we don’t explicitly encode it.

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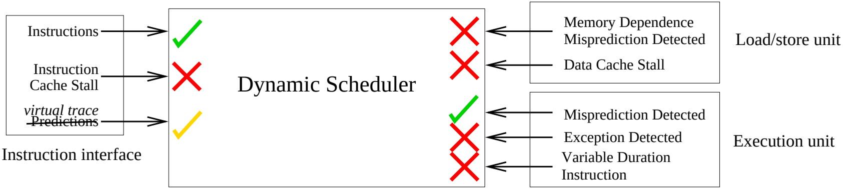
  - Chicken and egg problem!

J. Whitham and N. Audsley, Forming Virtual Traces for WCET Analysis and Reduction, Proc. RTCSA, 377–386, 2008.

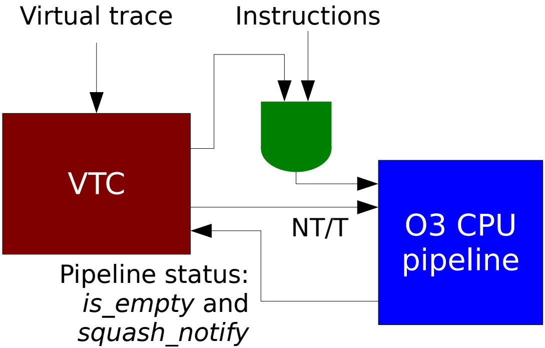
How virtual traces are implemented

(1) Sources of *timing noise* in O3 are constrained or eliminated:



How virtual traces are implemented

(2) The *virtual trace controller* (VTC) generates branch predictions and manages the flow of instructions into the pipeline:



Result: O3+VTC CPU: O3 with virtual trace extensions.

Experiment 1

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(b) a virtual trace CPU is used.

A subset of the Mälardalen benchmarks were executed within the following environments, measuring execution time:

- **IIO**: Idealized in-order CPU.
  Exactly one instruction executed every clock cycle.
- **O3+VTC**: Virtual trace CPU with maximum trace length $L \in [1, 20]$.

Results 1

	IIO	O3+VTC
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bubble	5,286	8,454
cnt	3,580	2,786
compress	3,545	4,093
crc	21,096	21,082
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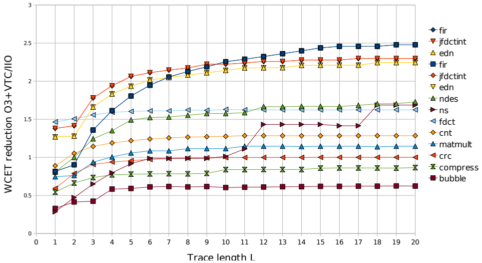

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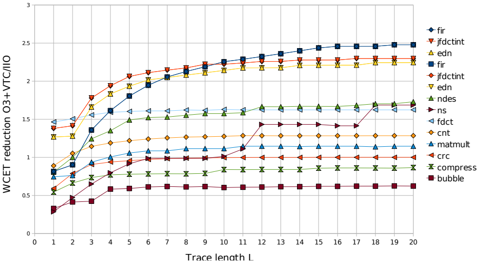
But available WCET reductions are highly dependent on program structure; unpredictable branches are a problem. *If-conversion* is a solution (localized single-path programming).



Experiment 2

> Q2: Which of the constraints needed to implement virtual traces have the greatest effect on execution time?

A subset of the Mälardalen benchmarks were executed within the following environments, measuring execution time. Each environment removes one of the constraints of O3+VTC:

- **O3+VTC-SYNC**: The pipeline is not resynchronized at trace end.
- **O3+VTC-SYNC-IOB**: Branches may be executed out of order.
- **O3+VTC-SYNC-SD**: Dynamic memory disambiguation is used.
- **O3+VTC-SYNC-NF**: Dynamic memory forwarding is permitted.

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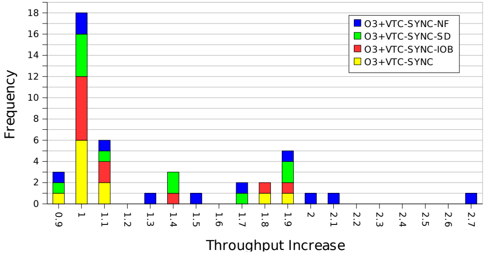
Unpredictable branches are only one problem! CPU constraints also increase C: O3+VTC is up to 3.6× slower than O3.



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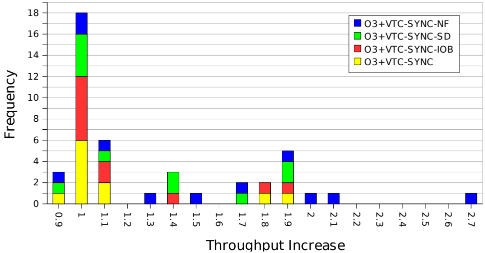

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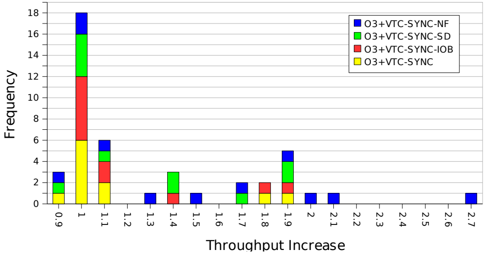
If only we could predict the addresses of loads and stores!



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- A scratchpad memory or locked cache would need to be used. Automatic data scratchpad allocation is *necessary* but *difficult*.

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A hard problem for general C code:

- Pointers can have almost any value.
- Memory might be allocated dynamically.

The same problems affect data cache modeling.

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The problem needs to be solved for typical C programs; otherwise, assumptions such as “perfect data cache” (as made in this work) will continue to be unrealistic.

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- The CPU constraints reduce the maximum performance but increase the guaranteed performance.
- Predictable management of data accesses is a problem that saps the performance of virtual traces.
- The automatic data scratchpad allocation problem must be solved.

End

- All questions and comments are welcome!
- You can find the O3+VTC experimental software on the web at `http://www.jwhitham.org.uk/c/vt.html`